What Is Claimed Is:

1. A liquid crystal display panel comprising:

first and second substrates;

a photo-hardening sealant between the first and second substrates;

a plurality of metal lines on the first substrate, wherein the metal lines are formed of a transparent conductive film at least at portions where the metal lines cross one another; and

a liquid crystal layer between the first and second substrates.

2. The panel of claim 1, wherein the metal lines include:

a plurality of gate lines in an active region;

a plurality of gate pads in a first pad region;

a plurality of data lines arranged to cross the gate lines; and

a plurality of data pads in a second pad region.

3. The panel of claim 2, further comprising a plurality of pad links connecting the gate lines and the gate pads, and the data lines and the data pads.

4. The panel of claim 3, wherein at least a portion of the pad links of the gate lines and the gate pads is formed of the transparent conductive film.

5. The panel of claim 3, wherein at least a portion of the pad links of the data lines and the data pads is formed of the transparent conductive film.

6. The panel of claim 1, wherein the transparent conductive film includes indium tin oxide (ITO).

7. A liquid crystal display panel comprising:

first and second substrates each having an active region and a pad region thereon;

a photo-hardening sealant along a boundary between the active region and the pad region;

a plurality of pads formed in the pad region;

a plurality of lines arranged to cross one another in the active region;

a plurality of pad links formed of a transparent conductive film connecting the pads and the lines; and

a liquid crystal layer between the first and second substrates.

8. The panel of claim 7, wherein the transparent conductive film includes ITO.

9. The panel of claim 7, wherein the pads include a plurality of gate pads each for receiving a gate driving signal from an external driving IC applied thereto and a plurality of data pads each for receiving a data signal from the external driving IC applied thereto.

10. The panel of claim 7, wherein the lines include a plurality of gate lines and a plurality of data lines, the gate lines and the data lines crossing one another, thereby defining a plurality of pixel regions.

11. The panel of claim 10, wherein the pixel regions include a pixel electrode.

12. The panel of claim 10, further comprising a thin film transistor at each crossing part of the gate lines and the data lines.

13. The panel of claim 9, further comprising a gate insulating film between the gate pads and the data pads.

14. The panel of claim 7, wherein the pad links include a gate pad link connecting the gate pad and the gate line and, a data pad link connecting the data pad and the data line.

15. The panel of claim 7, wherein the pad links include a plurality of gate pad links connected to the gate lines and a plurality of data pad links connected to the data lines.

16. A method for fabricating a liquid crystal display panel having an active region on a first substrate and first and second pad regions on a second substrate, the method comprising:

forming a plurality of gate lines at the active region and a plurality of gate pads at the first pad region;

forming a plurality of data lines at the active region between the gate lines and the gate pads and a plurality of data pads in the second pad region;

forming a plurality of pad links formed of a transparent conductive material connected between the gate lines and the gate pads, and the data lines and the data pads; and

attaching the first and second substrates.

17. The method of claim 16, further comprising forming a photo-hardening sealant along a circumference of the active region after forming the pad links.

18. The method of claim 16, further comprising injecting a liquid crystal after attaching the first and second substrates.

19. The method of claim 17, further comprising dropping a liquid crystal on the first substrate after forming a photo-hardening sealant.

20. The method of claim 16, further comprising:

forming a gate insulating film on the first substrate;

forming a semiconductor layer on the gate insulating film; and

forming source and drain electrodes on the semiconductor layer.

21. The method of claim 20, wherein the source and drain electrodes, the data lines, and the data pads are formed at the same time.

22. The method of claim 20, further comprising:

forming a protection film on the gate insulating film; and

forming a pixel electrode at the active region.

23. The method of claim 22, further comprising exposing the drain electrode, the gate pad, and the data pad after forming the protection film.

24. The method of claim 23, further comprising forming a transparent conductive film connecting the gate pad and the data pad after exposing the gate and data pads.

25. The method of claim 24, wherein the transparent conductive film and the pad links are formed at the same time.